**MAIN CONTROL DESIGN:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **O5** | **O4** | **O3** | **O2** | **O1** | **O0** | **RegDst** | **ALUSrc** | **MemtoReg** | **RegWrt** | **MemR** |
| **R-type** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| **lw** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| **sw** | 1 | 0 | 1 | 0 | 1 | 1 | X | 1 | X | 0 | 0 |
| **beq** | 0 | 0 | 0 | 1 | 0 | 0 | X | 0 | X | 0 | 0 |
| **bne** | 0 | 0 | 0 | 1 | 0 | 1 | X | 0 | X | 0 | 0 |
| **j** | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | 0 | 0 |
| **addi** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| **subi** | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

RegDst = O5’O4’O3’O2’O1’O0’

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **O5** | **O4** | **O3** | **O2** | **O1** | **O0** | **MemW** | **BEQ** | **BNE** | **JUMP** | **ALUOp1** | **ALUOp0** |
| **R-type** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **lw** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| **sw** | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| **beq** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **bne** | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| **j** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | X | X |
| **addi** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **subi** | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |